

# Design of PGA fully differential operational amplifier in CMOS image sensor

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**Abstract.** With the rapid development of CMOS image sensor, the research of dynamic range expansion technology has played an increasingly significant role in image processing. PGA is an important component used by CMOS image sensors to extend the dynamic range of systems which can change its voltage gain according to the sizes of images to extend the dynamic field. This paper includes a detailed description regarding to the basic structure of differential operational amplifiers embedded in PGA consists of two-stage common-source and common-gate circuits. Considering the stability of the system, a circuit applied a Miller compensation circuit with zero point control, a Common-mode-feedback circuit and a current mirror which was introduced to provide offset voltage for the operational amplifier. The manufacture of this kind of operational amplifier applies the UMC 110nm CMOS process, and the supply voltage of the amplifier is 3.3V. According to the results of simulation, the gain of the operational amplifier is 84.7dB; the phase margin is 71.6 degrees; the unity gain bandwidth is 102.5MHz; the differential output swing is  $\pm 2V$ ; the overall layout area is  $190\mu\text{m} * 100\mu\text{m}$ .

**Key words.** programmable gain amplifier; fully differential; common mode feedback; Miller compensation.

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## 1. Introduction

As the CMOS image sensor industry is developing so rapidly, foreign companies and research institutions have developed varieties of CMOS image sensors and Camera systems based on CMOS image sensor. Though these new products are hitting global markets constantly nowadays, the development of CMOS image sensor in our country starts is relatively lagging. Therefore, the research and manufacture of independent intellectual property rights, high performance and high value-added CMOS image products acquire a very significant implication.

Programmable gain amplifiers (PGA) have various structures and designs under the requirements of different image sensors. For instance, to meet the requirements of PGA with different structures, an operational amplifier was designed to adjust the bandwidth of OTA to improve the power consumption performance and the linearity of PGA by compensating capacitance [1]. Reference [2] puts forward another kind of operational amplifiers, which used an improved trans-conductance enhancement circuit to improve its trans-conductance enhancement capability and reduce the negative influence caused by the MOS drain source voltage variation. A design of low power switched capacitor PGA combines the operational amplifier sharing and dynamic biasing technology was illustrated in Reference [3]. It used the operational amplifier sharing technology to form the circuit structure to reduce the load effect. Reference [4,5] illustrates a programmable gain amplifier based on the thermometer code array set in an  $1024 * 1024$  CMOS image sensor. The system proposed in this paper adopts two level pipeline structure, which can make the design less complicated while efficiently improve the stability and accuracy of PGA system.

## 2. The main circuit structure of fully differential operational amplifier in PGA

### 2.1. Geometry of the plate

As the advantages and disadvantages have been listed in papers [6,7], we put forward a new internal structure of fully differential operational amplifier (Figure 1), consists a folded cascade structure used to increase the output swing and a common source amplifier.

The introduce of differential PMOS inputs can distinctly improve the operational amplifier secondary main pole frequency and reduce the noise. The common mode feedback circuit is able to narrow the current variation caused by the mismatch of the MOS transistor. As the sum of the current of the input tube PM1, PM2 and PM0 is different, the deviation will be increasingly obvious leading to the distortion of output signals. In the folded cascade tail current tube NM9, NM10 plus feedback signal to stabilize the output common mode voltage level. This structure simplified the extraction of common mode level, but increased power consumption[8,9].

By analyzing the operational amplifier gain, we can conclude that the gain of the

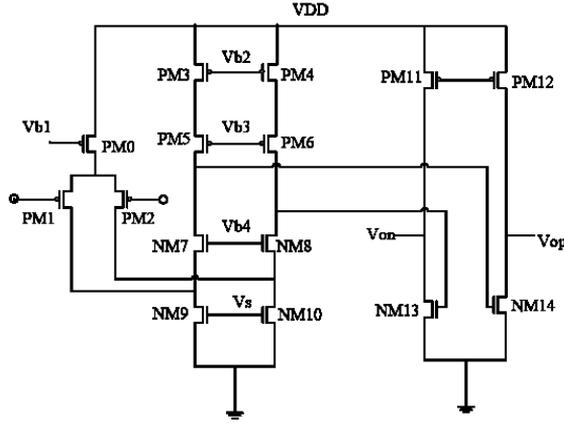


Fig. 1. The main operational structure

first folded cascode operational amplifier is:

$$K_0 = \mathbf{0}_{4 \times 4}, \quad m_0 = 0 \quad (1)$$

$$s = - \frac{g_{m1} g_{m7} g_{m5}}{g_{m5} g_{o7} (g_{o1} + g_{o9}) + g_{m7} g_{o5} g_{o3}} \quad (2)$$

Common source output gain:

$$\overline{\xi_D}(x_D, y_D) = \sum_{i=1}^M \sum_{j=1}^{2N} \overline{\xi_{D,i,j}}(x_D, y_D) \quad (3)$$

The gain of the entire circuit is:

$$A = A_1 * A_2 \quad (4)$$

Differential slew rate is the maximum output power of the amplifier when the input signal is large, defined as:

$$SR = \left. \frac{d_{vout}}{dt} \right|_{max} = \frac{I_{max}}{C} \quad (5)$$

Therefore, the overall conversion rate of the amplifier is:

$$SR = \min \{ I_{M0} / C_1, 2I_{M11} / (C_L) \} \quad (6)$$

## 2.2. Common mode feedback circuit

Because the fully differential common mode output voltage cannot be influenced by the negative feedback of differential signals, an extra loop is needed to determine the common mode output voltage level. The output common mode voltage levels

of high gain amplifiers are so sensitive to device characteristics and its mismatch that the detection of common mode voltage levels by using common mode feedback sampling structure in the network is necessary. It will be compared to the reference voltage thereafter and the bias voltage of amplifiers will be readjusted according to the results of the comparison. The common mode feedback network is designed to stabilize the output voltage of the fully differential circuit and improve the common mode rejection ratio [10-12].

In the Figure 2 below a sampling circuit containing the requirements listed above adopts sampling resistances and a feedback circuit is also applied for feedback sampling. The common mode detection resistor is 10K?, which is able to limit the current difference between the output ends and guarantee the sensitivity of the differential output voltage detection.

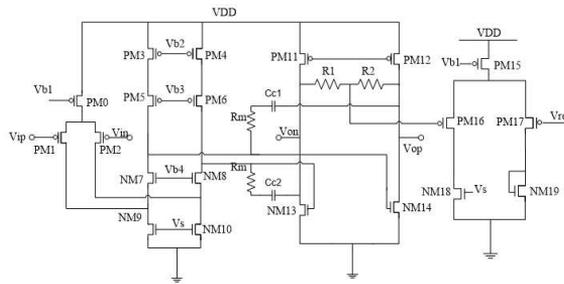


Fig. 2. The full differential operational amplifier circuit diagram

(1)Open loop gain

Based on the previous analysis, it is assumed that the accuracy of each circuit is the same, then  $V_{in}(1 - \epsilon_{A1})A_1 \cdot (1 - \epsilon_{A2})A_2 = (1 - 0.1\%)A_1 \cdot A_2 \cdot V_{in}$ ,

We can calculate the accuracy error of each level of PGA to achieve the accuracy of the error:

$$(1 - \frac{1}{FA_v}) > 0.9995 \Rightarrow A_v \geq 76.22dB$$

(2)Unity gain bandwidth

As the output error of each level is about 0.05% on average, a formula is established to approximate the signal of the closed-loop system:  $1 - e^{-\frac{t}{\tau}} < 0.9995 \Rightarrow t \approx 7.5\tau$  Thus in order to meet the requirement of accuracy, a  $7.5\tau$  is needed to achieve system stability (t is the closed loop time constant). Because of the large variation of feedback coefficient of PGA which has negative impacts on the bandwidth, we decided the sampling and amplification of the clock period to be 400ns while the small signal stability time is 200ns.

$$7.5\tau = 200ns \Rightarrow w = \frac{1}{\tau} = \frac{7.5}{200ns} \Rightarrow f = \frac{w}{2\pi} = 6MHz$$

In a full differential operational amplifier, the open loop bandwidth  $BW=f/F$  approximately, (F is the feedback coefficient); while in the PGA presented in this paper, the minimum feedback coefficient is 0.3, so the unity gain bandwidth can be figured

out:  $GBW = \frac{f}{F} > 20MHz$

As the feedback coefficient of this PGA system is relatively smaller while its variation and the impacts it impose on the bandwidth is relatively larger, the operational amplifier open loop gain bandwidth should be far greater than 20MHz.

### 3. Simulation and layout of OPERATIONAL AMPLIFIER in PGA circuit

PGA is an important part of CMOS image sensors, which is composed of digital analog hybrid circuits. Before engaging in the circuit layout, all stages in the circuit must be guaranteed that their functions are correctly arranged and achievable. The parasitic effects of capacitance and resistance are majorly considered because of the low operating frequency acquired by the programmable gain amplifier presented in this paper. In order to reduce this parasitic effect, parameters of the line width of the wire connected to the power supply and ground were introduced. For large current conductors, we used multilayer parallel lines to reduce the parasitic effect. Besides, contact holes of the substrate and the substrate were also added in the vicinity of the active region of the MOS tube connected to the power supply in preventing the latch up effect.

Figure 3 displays the overall circuit layout of the operational amplifier in PGA, covering an area of 190um \* 100um.

Figure 4 is the simulation curve of amplitude frequency and phase frequency characteristics of our fully differential operational amplifier. Obviously the gain, phase margin and unity gain bandwidth of the operational amplifier is 84.7dB, 71.6 degrees and 102.5MHz respectively.

Other parameters of the operational amplifier are also post simulated, and the results of the pre simulation and post simulation are listed together in table 1. Generally these figures are still perfectly content the design requirements.

The Figure 5 illustrates the post simulation results of the 0~15dB gain sampling process of the PGA within the corresponding switching timing, with conditions including 1.4V and 1.6V input signals and scanning range covering 0-15u. As the output simulation curve shows, the exponential variation function is fully guaranteed by the differential output voltage difference.

### 4. Conclusion

In this paper, we put forward a fully differential operational PGA design based on CMOS image sensor, which adopted two stage cascade circuit structure. The Miller compensation circuit, common mode feedback circuit with zero control and the current mirror technology are also introduced to improve the stabilization of the system. The operational amplifier applies UMC 110nm CMOS process and uses 3.3V voltage supply, while acquiring a differential output swing of  $\pm 2V$ . By simulating the circuit we have recorded that the gain of the operational amplifier is 84.7dB, the phase margin is 71.6 degrees, the unity gain bandwidth is 102.5MHz, and the overall

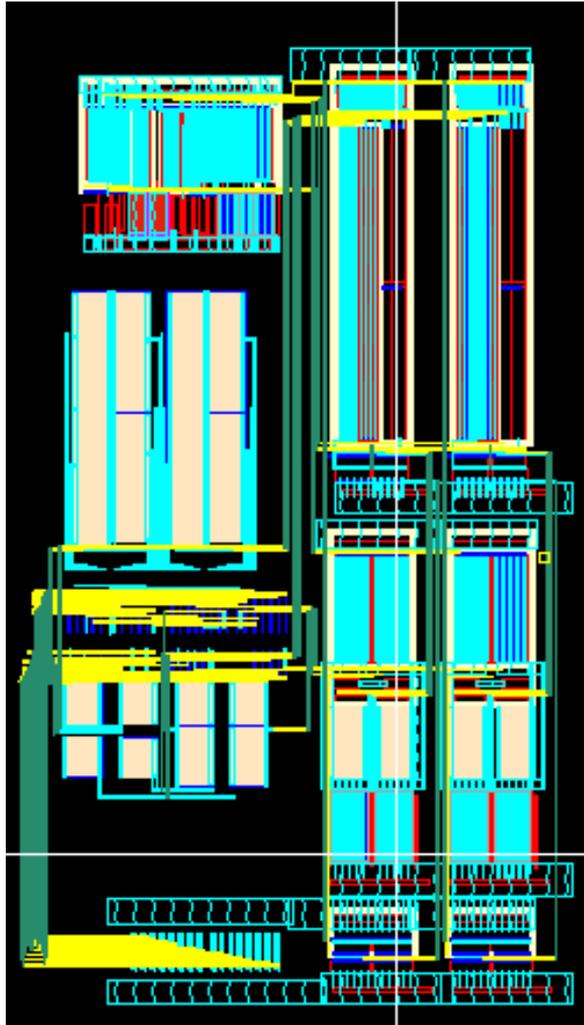


Fig. 3. The CMOS image sensor layout based on PGA

layout area is  $190\mu\text{m} * 100\mu\text{m}$ , which proved that the performance of this operational amplifier can utterly meet the system requirements.

## References

- [1] QIN. YONGYUAN, YAN . ONGMIN, GU DONGQING: *A Clever Way of SINS Coarse Alignment despite Rocking Ship*. Journal of Northwestern Polytechnical University 23 (2005), No. 5, 681–684.
- [2] ZHAO. SHUANG, LIU. YUNTAO: *Design of a CMOS Rail-to-Rail Operational Amplifier with constant transconductance*. Microelectronics 46 (2016), No. 3, 302–305.

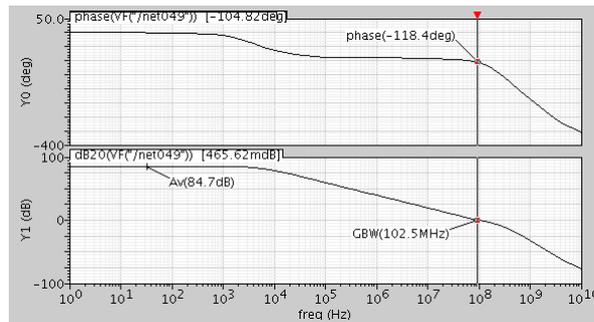


Fig. 4. The post-simulation of amplitude-frequency characteristic and phase frequency response

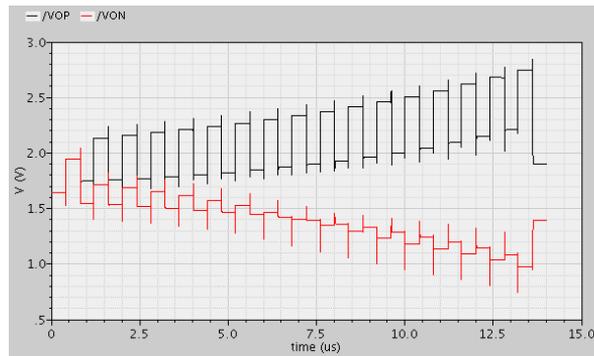


Fig. 5. The transient post-simulation results of PGA

- [3] HE. ZEWEL, GUO. JUN, ZHANG. GUO. JUN: *Design of a High CMRR High Gain Operational Amplifier*. *Microelectronics* 45 (2015), No. 4, 457–460.
- [4] LIAN. JUNXIANG, TANG. YONGGANG, WU. MEIPING: *Study on SINS Alignment Algorithm with Inertial Frame for Swaying Bases*. *Journal of National University of Defense Technology* 29 (2007), No. 5, 93–97.
- [5] TANG. NING, YANG. QIUYU, ZHAI. JIANGHUI: *Design of High performance fully differential Operational Amplifier*. *Microelectronics* 41 (2011), No. 5, 636–639.
- [6] SONG. QIWEI, ZHANG. ZHENGPING: *Design of a novel high-speed fully-differential CMOS op-amp*. *Modern Electronics Technique* 35 (2012), No. 4, 166–172.
- [7] NAGASE, KOICHI, WADA: *A Demonstration of TIA Using FD-SOI CMOS OPAMP for Far-Infrared Astronomy*. *Journal of Low Temperature Physics* 184 (2016), No. 2, 449–453.
- [8] DE. MATTEIS. M, DONNO. A, D. AMICO. S: *0.9 V third-order 132 MHz single-OPAMP analogue filter in 28 nm CMOS*. *Electronics Letters* 53 (2017), No. 2, 77–79.
- [9] SUTULA. S, DEI. M, TERES. L: *Class-AB single-stage OpAmp for low-power switched - capacitor circuits*. *IEEE International Symposium on Circuits and Systems* (2015), 2081–2084.
- [10] TAMADDON, MOHSEN, YAVARI: *High-performance time-based continuous-time sigma-delta modulators using single-opamp resonator and noise-shaped quantizer*. *Microelectronics Journal* 56 (2014), 110–121.
- [11] EL. SAYED, SARAH. A. FAHMY, GHAZAL. A: *A low power sigma-delta modulator using charge-steering Opamp for Bluetooth application*. *Canadian Conference on Electrical and Computer Engineering* (2015), 1184–1187.

- [12] JIANG, Y. F: *Error analysis of analytic coarse alignment*. IEEE Transactions on Aerospace and Electronic Systems 34 (1998), No. 1, 334-337.

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